

WHAT IS CLAIMED IS:

1. A data transfer device which is connected to first and second buses and transfers data between these buses, wherein the device can independently request a bus access right and output an address to the first and second buses, and the device requests a bus access right of one bus for reading and requests a bus access right of the other bus for writing in response to one data transfer start request.
2. The data transfer device according to claim 1, wherein the device requests a bus access right of the one bus and requests a bus access right of the other bus at different timings.
3. The data transfer device according to claim 2, wherein the device requests a bus access right of the one bus at a predetermined timing for read operations of the other bus granted a bus access right.
4. The data transfer device according to claim 3, wherein a plurality of data transfer channels and a control register to specify data transfer channel operations are provided, and wherein the control register has a transfer request generation source specification area for defining correspondence between a data transfer channel to receive a transfer request and a transfer request generation source; a source bus specification area for defining correspondence

between a data transfer channel and a transfer source bus; and a destination bus specification area for defining correspondence between a data transfer channel and a transfer destination bus.

5. A semiconductor integrated circuit comprising:

- a first bus;
- a second bus;
- a data transfer device to transfer data between the first and second buses;
- a central processing unit connected to the first bus;

and

program storage memory which stores a control program for the central processing unit and is connected to the first bus,

wherein the data transfer device can independently request a bus access right and output an address to the first and second buses, the device requests a bus access right of one bus for reading and requests a bus access right of the other bus for writing at a different timing in response to one data transfer start request, and

wherein the central processing unit is capable of bus access using the first bus in parallel with bus access using the second bus by means of the data transfer device.

6. A semiconductor integrated circuit comprising:

- a first bus;

a second bus;

a data transfer device to transfer data between the first and second buses;

a central processing unit connected to the first bus;

and

a bus control means for the first and second buses, wherein the data transfer device can independently request a bus access right and output an address to the first and second buses, the device requests a bus access right of one bus for reading and requests a bus access right of the other bus for writing at a different timing in response to one data transfer start request, and

wherein the bus control means is capable of arbitration of bus access right requests and bus control for the first and second buses independently.

7. A semiconductor integrated circuit comprising:

a first bus;

a second bus;

a third bus;

a central processing unit connected to the first bus;

program storage memory which stores a control program for the central processing unit and is connected to the first bus; and

a data transfer device capable of data transfer between the second and third buses,

wherein the data transfer device can independently request a bus access right and output an address to the second and third buses, the device requests a bus access right of one bus for reading and requests a bus access right of the other bus for writing at a different timing in response to one data transfer start request, and

wherein the central processing unit is capable of bus access using the first bus in parallel with bus access using the second or third bus by means of the data transfer device.

8. The semiconductor integrated circuit according to claim 7 including a bus control means for the first through third buses,

wherein the bus control means is capable of arbitration of bus access right requests and bus control for the first through third buses independently.

9. The semiconductor integrated circuit according to claim 8,

wherein the central processing unit can access the second or third bus from the first bus via the bus control means.

10. A microcomputer comprising:

a first bus;

a second bus;

a third bus;

a central processing unit connected to the first bus; program storage memory which stores a control program

for the central processing unit and is connected to the first bus; and

a data transfer device capable of data transfer between any two of the first through third buses,

wherein the data transfer device can independently request a bus access right and output an address to the first through third buses, and the device requests a bus access right of one bus for reading and requests a bus access right of the other buses for writing at a different timing in response to one data transfer start request.

11. The microcomputer according to claim 10,

wherein the central processing unit is capable of bus access using the first bus in parallel with bus access using the second or third bus by means of the data transfer device.

12. The microcomputer according to claim 11 including a bus control means for the first through third buses,

wherein the bus control means is capable of arbitration of bus access right requests and bus control for the first through third buses independently.

13. The microcomputer according to claim 12,

wherein the central processing unit can access the second or third bus from the first bus via the bus control means.

14. The microcomputer according to claim 10,

wherein the data transfer device has a plurality of data transfer channels and a control register to specify data

transfer channel operations, and

wherein the control register has a transfer request generation source specification area for defining correspondence between a data transfer channel to receive a transfer request and a transfer request generation source; a source bus specification area for defining correspondence between a data transfer channel and a transfer source bus; and a destination bus specification area for defining correspondence between a data transfer channel and a transfer destination bus.

15. The microcomputer according to claim 14,
wherein a central processing unit can access the
control register.